FPGAs, CPUs, DRAM, or communications: who's the technology driver?

Ron Wilson - November 02, 2006

Which application really drives process technology? Once upon a time everyone agreed that DRAM, with its need for the smallest critical dimensions, lowest defect densities and lowest cost, drove CMOS processes. But DRAM processes diverged so far from logic CMOS that they are now hardly relevant. Intel and AMD are similar in that regard. Their focus on clock speed, their reliance on custom design and the single-product nature of their fabs makes them more of a special case than a process driver, even though they continue to push the envelope in critical dimensions.

This has left FPGAs to claim the title. Certainly in many cases the first volume product through certain foundries at a new process node will be from either Altera or Xilinx. FPGAs exercise not only fast logic but also SRAM speed and density, and the whole interconnect stack. What's more, since they can be configured to self-diagnose, they can locate failure sites on the wafer, and hence are ideal tools for wringing out systematic logic yield issues in a new process. But they are also highly regular arrays of tiny hand-crafted blocks, and not very rich in analog circuits. They may be best-, rather than worst-case scenarios for OPC and pattern-sensitive process issues.

At the Savant SoC Conference in Newport Beach yesterday, keynote speaker Mehdi Hatamian, VP engineering for DSP microelectronics at Broadcom, made an interesting argument that it is really communications SoCs that are driving general process technology today. He pointed out that today's communications chips can include demanding Gigabit or even 10 Gigabit PHY blocks, perhaps RF circuitry, and a huge variety of digital IP. They must not only support fast I/O, but preserve the bandwidth of data flows all the way through the chip from input to output, stressing logic and RAM speed as well as interconnect. They cannot depend on repeating hand-crafted regular patterns, but must live with a cell-based methodology, at least some third-party design tools and hence a highly irregular layout. And they must achieve this within power constraints that would be unthinkable for an FPGA.

Are communications SoCs the new process driver? Broadcom decided to skip over 90 nm to go directly to 65 nm for its new designs. That move will probably make Broadcom chips the first SoC-type designs to hit some new process nodes. And Broadcom's designs present the whole spectrum of problems that the foundry will eventually see as it engages with other SoC customers, rather than the restricted special case presented by FPGAs. Maybe there's a case to be made there.